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**BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES**

Application Number: 10/714,031

Filing Date: November 14, 2003

Appellant(s): HUBIS, WALTER

Daniel Fishman, Reg.No. 35512
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 06/12/2008 appealing from the Office action mailed 01/04/2008.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

Mullendore	US Publication 2003/0185154	October 2, 2003
Liu, Wei et al.	US Publication 2004/0117441	June 17, 2004

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-6,11, 15,18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mullendore et al. (US Publication 2003/0185154) further in view of what was well-known in the art.

Mullendore disclosed (re. Claim 1) a storage network appliance comprising: a TCP/IP router for routing block level storage requests through a TCP/IP network communication medium; (Mullendore-Paragraph 72, Figure 7) and a cache memory for caching storage data blocks accessed by the block level storage requests. (Mullendore-Paragraph 72, Figure 7)

Mullendore disclosed (re. Claim 1) wherein the cache memory is used by the router to store data blocks exchanged between the first and second devices through the router, (Mullendore-Paragraph 72, Figure 7)

While Mullendore substantially disclosed the claimed invention Mullendore did not disclose (re. claim 1) wherein the cache memory is used to return data blocks from the cache memory to the first device in response to a received block level storage request directed from the first device to read data blocks from the second device without forwarding the storage request to the second device.

At the time of the invention it would have been well-known in the networking art that if a request for data is satisfied by a cache then there would be no need to forward said request for data. At time of the invention it would have been obvious to person of ordinary skill in the networking art to combine what was well-known in the art into Mullendore. The motivation for said combination would have been to improve data retrieval processing using cache storage.

Mullendore disclosed (re. Claim 2) a command and response processor coupled to the router for interpreting block level storage requests (Mullendore-Paragraph 70)

routed through the router and coupled to the cache memory for caching data identified in the interpreted block level storage requests.

Mullendore disclosed (re. Claim 3) wherein the block level storage requests are iSCSI protocol commands and responses. (Mullendore-Paragraph 13)

Mullendore disclosed (re. Claim 4) wherein the command and response processor is a SCSI command and response processor. (Mullendore-Paragraph 13)

Mullendore disclosed (re. Claim 5) wherein the command and response processor is adapted to snoop the block level storage requests routed by the router. (Mullendore-Paragraph 45)

Mullendore disclosed (re. Claim 6) wherein the router is adapted to store and forward received requests. (Mullendore-Paragraph 72, Figure 7)

Mullendore disclosed (re. Claim 11) a method operable in a network router

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comprising the steps of: receiving a block level storage request from a network communication medium; and processing the received block level storage request in association with a cache memory local to the router. (Mullendore-Paragraph 72, Figure 7)

Mullendore disclosed (re. Claim 11) responsive to receipt of a block level storage request from the first device to return data from the second device, locating data requested by the received block level storage request in the cache memory; returning the located data to a requesting first device in response to locating the requested data; and conditionally forwarding the received request to the second device only in response to failure to locate the requested data in the cache memory.

At the time of the invention it would have been well-known in the networking art that if a request for data is satisfied by a cache then there would be no need to forward said request for data. At time of the invention it would have been obvious to person of ordinary skill in the networking art to combine what was well-known in the art into Mullendore. The motivation for said combination would have been to improve data retrieval processing using cache storage.

Mullendore disclosed (re. Claim 15) an iSCSI router comprising: an inbound network interface for receiving iSCSI storage requests and for returning responses to

received iSCSI storage requests; (Mullendore-Paragraph 72, Figure 7)

an outbound network interface for forwarding received iSCSI requests to a destination device and for receiving responses from the destination device; (Mullendore-Paragraph 72, Figure 7)

a cache memory; (Mullendore-Paragraph 72, Figure 7) and a control element coupled to the inbound network interface, coupled to the outbound network interface, (Mullendore-Paragraph 72, Figure 7) and coupled to the cache memory and adapted to process iSCSI requests received on the inbound network interface in association with the cache memory and adapted to selectively forward processed iSCSI requests to a destination device via the outbound network interface.

(Mullendore-Paragraph 72, Figure 7)

Mullendore disclosed (re. Claim 15) wherein the cache memory is used by the control element to store data blocks exchanged between a first device coupled to the inbound network interface and a second device coupled to the outbound network interface, and wherein the cache memory is used to return data blocks from the cache memory to the first device in response to a received block level storage request directed from the first device to read data blocks from the second device without forwarding the storage request to the second device.

At the time of the invention it would have been well-known in the networking art that if a request for data is satisfied by a cache then there would be no need to forward said request for data. At time of the invention it would have been obvious to person of ordinary skill in the networking art to combine what was well-known in the art into Mullendore. The motivation for said combination would have been to improve data retrieval processing using cache storage.

Mullendore disclosed (re. Claim 18) an improved network router compatible with TCP/IP protocols and adapted for coupling to one or more host systems and one or more iSCSI compatible storage devices, the improvement comprising: a SCSI command and response processor (Mullendore-Paragraph 13) within the router to process iSCSI commands and responses forwarded through the router; and a cache memory within the router (Mullendore-Paragraph 72, Figure 7) coupled to the SCSI command processor for caching data related to iSCSI commands and responses processed by the SCSI command and response processor.

Mullendore disclosed (re. Claim 18) wherein the SCSI command and response processor is adapted to conditionally forward received iSCSI commands to a storage device based on processing of the iSCSI command in association with the cache memory. (Mullendore-Paragraph 72, Figure 7)

Mullendore disclosed (re. Claim 18) wherein the SCSI command and response processor is adapted to process iSCSI read requests by first attempting to locate requested data in the cache memory and wherein received iSCSI read requests are forwarded to a storage device only if the requested data is not located by the processor in the cache memory.

At the time of the invention it would have been well-known in the networking art that if a request for data is satisfied by a cache then there would be no need to forward said request for data. At time of the invention it would have been obvious to person of ordinary skill in the networking art to combine what was well-known in the art into Mullendore. The motivation for said combination would have been to improve data retrieval processing using cache storage.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

Art Unit: 2144

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7,10,13,17,21,22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mullendore et al. (US Publication 2003/0185154) further in view of Liu, Wei et al. (US Publication 2004/0117441).

While Mullendore substantially disclosed the claimed invention Mullendore did not disclose (re. Claim 7) wherein the command and response processor is adapted to process received requests while the requests are temporarily stored for forwarding.

Mullendore did not (re. Claim 10) wherein the command and response processor is adapted to coalesce multiple block level storage write requests into a coalesced block level storage write request and wherein the router is adapted to forward the coalesced block level write request to a destination device in place of the multiple block level storage write requests.

Liu disclose (re. Claim 7) wherein the command and response processor is adapted to process received requests while the requests are temporarily stored for forwarding. (Liu-Paragraph 9,Paragraph 118)

Liu disclosed (re. Claim 10) wherein the command and response processor is adapted to coalesce multiple block level storage write requests into a coalesced block

level storage write request and wherein the router is adapted to forward the coalesced block level write request to a destination device in place of the multiple block level storage write requests. (Liu-Paragraph 9,Paragraph 118)

Mullendore and Liu are analogous art because they present concepts and practices regarding routing of iSCSI write requests using a router cache. At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine Liu into Mullendore. The motivation for said combination would have been (Liu-Paragraph 4) to improves the data transmit characteristics between local and remote storage.

Mullendore-Liu disclosed (re. Claim 13, 17) coalescing multiple received block level storage requests into a coalesced block level storage request; and forwarding the coalesced block level storage request to a destination device. (Liu-Paragraph 9,Paragraph 118)

Mullendore-Liu disclosed (re. Claim 21) wherein the SCSI command and response processor is adapted to process iSCSI write requests by storing the associated write data in the cache memory. (Liu-Paragraph 9,Paragraph 118)

Mullendore-Liu disclosed (re. Claim 22) wherein the SCSI command and response processor is further adapted to coalesce data stored in the cache memory into

a larger coalesced write request and is further adapted to route the coalesced write request to the storage device. (Liu-Paragraph 9,Paragraph 118)

(10) Response to Argument

The Applicant presents the following argument(s) [*in italics*]:

... While Applicant admits that Mullendore uses the word "cache" he provides no explanation of its function other than as a buffer to hold data in far-end switch 240

...Mullendore teaches nothing more than a simple buffer for "speed matching" ...

The Examiner respectfully disagrees with the Applicant.

The Applicant appears to be differentiating a cache from buffer memory and indicates that a buffer memory cannot be used for cache storage. The Examiner notes that the Applicant Specification Page 9 Lines 5-10 indicate claimed invention as being embodied by a cache buffer memory for locating data within the cache buffer memory in expedited fashion. Thus the Examiner maintains there is no distinction between the claimed invention and Mullendore's router cache.

The Applicant presents the following argument(s) [*in italics*]:

... Nothing in Mullendore teaches the complexity of a router that processes the

block level storage requests exchanged between a first and second iSCSI device coupled through the router...

The Examiner respectfully disagrees with the Applicant.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., '*complex requests*') are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims.

The Applicant presents the following argument(s) [*in italics*]:

There is no art provided by the Examiner or any suggestion in the art to apply cache memory management techniques and structures within a network appliance router (a TCP/IP router). As noted, Mullendore suggest nothing more than well-known speed-matching buffer...

The Examiner respectfully disagrees with the Applicant.

The Applicant Specifications Page 3 indicates well-known caching techniques such that subsequent requests for the same data may be satisfied by the cache buffer memory.

Where Mullendore disclosed caching the data in the router, it would have been obvious to incorporate well-known caching techniques in said cache.

The Applicant presents the following argument(s) [*in italics*]:

Applicant responds that use of a cache in other contexts to speed read request processing is generally known in the art and is admitted in the Background section of the subject application. For example, processors and storage devices/systems use such caching techniques. However, such caching is not known in the art of network appliances and in particular iSCSI routers...

The Examiner respectfully disagrees with the Applicant.

The Examiner notes that the Applicant network appliances refer to well-known devices such as hubs, switches, and routers. (Applicant Specification Page 3)

The Examiner respectfully maintains that at the time of the invention caching as implemented in routers was well-known in the networking art. (See Terrell, US Patent 7200144 Column 6 Lines 30-55; See DiCorpo US Publication 2004/0139240 Paragraph 16; See Kuik US Patent 7188194 Column 4 Lines 10-35; See Dropps US Publication 2005/0044267 Paragraph 36)

Furthermore the Applicant has not presented evidence indicating how it would have been difficult to implement a cache in iSCSI routers as compared to the routers described in the prior art shown above.

Where Mullendore disclosed caching the data in the router, it would have been obvious to incorporate well-known caching techniques in said cache.

At the time of the invention it would have been well-known in the networking art that in context of cache operations if a request for data is satisfied by a cache then there

would be no need to forward said request for data to an alternate storage device and that the cache copy of the data will be sent in response to said request. At time of the invention it would have been obvious to person of ordinary skill in the networking art to combine what was well-known in the art into Mullendore. The motivation for said combination would have been to improve data retrieval processing using cache storage.

Furthermore (re. Claim 1) in response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., *iSCSI routers*) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims.

The Applicant presents the following argument(s) [*in italics*]:

...it is only through improper hindsight applying the teachings of the subject application that the Examiner asserts this "well-known" knowledge.

The Examiner respectfully disagrees with the Applicant.

In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/G. B./

/Paul H Kang/

Primary Examiner, Art Unit 2144

/William C. Vaughn, Jr./

Supervisory Patent Examiner, Art Unit 2144

Conferees:

/William C. Vaughn, Jr./

Supervisory Patent Examiner, Art Unit 2144